



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,212	11/12/2003	Michael E. Connell	2269-5083.1US (01-0428.01)	6326
24247	7590	01/02/2009	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			LEE, EUGENE	
			ART UNIT	PAPER NUMBER
			2815	
			NOTIFICATION DATE	DELIVERY MODE
			01/02/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

Office Action Summary	Application No.	Applicant(s)	
	10/706,212	CONNELL ET AL.	
	Examiner	Art Unit	
	EUGENE LEE	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 September 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8,10-14,16-20 and 22-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8,10-14,16-20 and 22-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 November 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>10/16/08</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: element 34 (Fig. 10). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 2, 4-8, 10-14, 16-20, and 22-24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains

Art Unit: 2815

subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The limitation “the passivation layer including silicon dioxide and silicon nitride” is not described in the specification. In paragraph [0054], the applicant only states that “Passivation layer 40 may comprise any of a variety of materials, including silicon dioxide and silicon nitride as examples”, however, the applicant does not state that the passivation layer may be a combination of these materials. Further, the same paragraph details silicon dioxide singularly without any mention of silicon nitride used in combination.

4. Claims 1, 2, 4-8, 10-14, 16-20, and 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear whether the limitation “passivation layer including silicon dioxide and silicon nitride” means a passivation layer having both silicon dioxide and silicon nitride or a passivation layer having either/or silicon dioxide and silicon as described by the applicant’s specification. Appropriate clarification and/or correction are required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

Art Unit: 2815

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. In view of the 112 rejection above, claims 1, 7, 13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginn et al. 5,827,771 in view of Ishikawa USPGPubs 2002/0064930.

Regarding claims 1, 7, 13 and 19, Figure 2 of Ginn discloses a semiconductor die comprising: a semiconductor substrate 12 having a front side 12c and a back side 12b, a low ratio of height to horizontal dimension (see fig. 2), tensile stresses, and compressive stresses; an integrated circuit (IC) on a portion 14 of the front side; and a stress-balancing layer 18 covering at least a portion of the backside. Ginn does not explicitly disclose a passivation layer covering a portion of the IC. Figure 1 of Ishikawa discloses a SiN passivation layer 3 (paragraph [0045]) formed on an IC chip 1. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Ginn by including a SiN passivation layer on the IC portion for the purpose of protecting the circuitry in layer 14. After the combination, the SiN passivation layer will inherently exert at least a small amount of stress (either tensile or compressive) on the substrate. The SiN stress-balancing layer 18 will inherently balance the small amount of additional stress imparted by the passivation layer. Note that a compressive stress in a first direction (e.g., vertical) creates a tensile stress in a direction perpendicular to the first direction (e.g., horizontal) (and vice versa). Therefore, the substrate has both compressive and tensile stresses.

Regarding claims 2, 8, 10, 14, 16, 20 and 22, Ginn teaches that the balancing layer 18 is a SiN film, which may be considered a single component layer. The limitations "sensitive to an

Art Unit: 2815

optical energy altering the material by at least one of heating..." and "for laser-marking" are merely recitations of intended use that do not structurally distinguish the claimed invention over the prior art. The balancing layer is capable of being modified (marked) by laser beam.

7. Claims 5, 6, 11, 17, 23, and 24 rejected under 35 U.S.C. 103(a) as being unpatentable over Ginn in view of Ishikawa as applied to claims 1, 7, 13, and 19 above, and further in view of Sakaki et al. (US PGPub 2003/0017652, hereinafter Sakaki).

Regarding claims 5, 6, 11, 17, 23 and 24, Ginn does not disclose an adhesive layer attached to the stress balancing layer. Sakaki teach in figure 9 an adhesive layer 41A attached to a stress-balancing layer 2 (para. 0136). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Ginn by including the adhesive layer of Sakaki for the purpose of mounting the IC chip to a support structure. The limitation "sensitive to an optical energy altering the material by at least one of heating..." are merely recitations of intended use that do not structurally distinguish the claimed invention over the prior art. The adhesive material is capable of being modified (marked) by laser beam.

8. In view of the 112 rejection above, claims 1, 2, 7, 8, 10, 13, 14, 16, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao (US Pat. 6,277,725) in view of Sakaki.

Art Unit: 2815

Regarding claims 1, 7, 13, and 19, Figure 1A of Hsiao discloses a semiconductor die comprising: a semiconductor substrate 100 having a front side (top) and a back side (bottom), a low ratio of height to horizontal dimension, tensile stresses, and compressive stresses; an integrated circuit (IC) on a portion 14 of the front side; and a passivation layer 104/106 covering a portion of the IC causing a stress on at least a portion of the substrate (inherent), the passivation layer including silicon dioxide (layer 104) and silicon nitride (layer 106) (col. 2, lines 34-36). Hsiao does not specifically disclose a stress-balancing layer formed on the back side of the substrate to balance the stress caused by the passivation layer. Figure 3 of Sakaki discloses an IC device with a stress-balancing layer 2 balancing the stress caused by an overlying passivation layer 7 (see paragraphs [0106] and [0107], esp. [0107] at the third sentence, which teach that layer 7 causes a stress which is compensated by layer 2). Sakaki further teaches that the passivation layer 7 and the stress-balancing layer 2 are made of the same material (thermosetting resin) (paragraphs [0105] and [0107]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Hsiao by including a stress-balancing layer made of the same materials as the passivation layer (as taught by Sakaki) for the purpose of preventing substrate warping, as is known in the art. Furthermore, it has been held that using a known technique to improve similar devices in the same way would have been obvious. *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007). Note that a stress balancing layer made of the same materials as the passivation layer (SiO and SiN) of Hsiao could have been deposited by CVD.

Regarding claims 2, 8, 10, 14, 16, 20 and 22, after the above combination, Hsiao in view of Sakaki teach that the balancing layer comprises a SiN film, which may be considered a single

Art Unit: 2815

component layer. The limitations "sensitive to an optical energy altering the material by at least one of heating..." and "for laser-marking" are merely recitations of intended use that do not structurally distinguish the claimed invention over the prior art. The balancing layer is capable of being modified (marked) by laser beam.

9. In view of the 112 rejection above, claims 1, 2, 7, 8, 10, 13, 14, 16, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao (US Pat. 6,277,725) in view of Ouellet et al. (US PGPub 2002/0064359).

Regarding claims 1, 7, 13, and 19, Figure 1A of Hsiao discloses a semiconductor die comprising: a semiconductor substrate 100 having a front side (top) and a back side (bottom), a low ratio of height to horizontal dimension, tensile stresses, and compressive stresses; an integrated circuit (IC) on a portion 14 of the front side; and a passivation layer 104/106 covering a portion of the IC causing a stress on at least a portion of the substrate (inherent), the passivation layer including silicon dioxide (layer 104) and silicon nitride (layer 106) (col. 2, lines 34-36). Hsiao does not specifically disclose a stress-balancing layer formed on the back side of the substrate to balance the stress caused by the passivation layer. Figure 2b of Ouellet a substrate 1 with a passivation layer 3 on a top surface of the substrate and a stress-balancing layer 3 on the bottom surface, wherein the stress-balancing layer balances the stress caused by the overlying passivation layer 2 (see abstract). Ouellet further teaches that the passivation layer and the stress-balancing layer are made of the same material (silica) (paragraphs [0030] and [0031]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify

Art Unit: 2815

the invention of Hsiao by including a stress-balancing layer made of the same materials as the passivation layer (as taught by Ouellet) for the purpose of preventing substrate warping.

Furthermore, it has been held that using a known technique to improve similar devices in the same way would have been obvious. *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007). Note that a stress balancing layer made of the same materials as the passivation layer (SiO and SiN) of Hsiao could have been deposited by CVD.

Regarding claims 2, 8, 10, 14, 16, 20 and 22, after the above combination, Hsiao in view of Ouellet teach that the balancing layer comprises a SiN film, which may be considered a single component layer. The limitations "sensitive to an optical energy altering the material by at least one of heating..." and "for laser-marking" are merely recitations of intended use that do not structurally distinguish the claimed invention over the prior art. The balancing layer is capable of being modified (marked) by laser beam.

Response to Arguments

10. Applicant's arguments filed 9/16/08 have been fully considered but they are not persuasive.

Regarding the 112 rejection, see above.

Regarding the applicant's argument that Ginn in view of Ishikawa does not teach or suggest all the claim limitations of the claimed invention, this argument is not persuasive because the references do indeed teach all of the claimed structural limitations. Ginn discloses (see, for example, Figure 2) a semiconductor die comprising a substrate 12, circuit layer

Art Unit: 2815

(integrated circuit) 14, and stress-balancing layer 18. Ginn does not disclose the passivation layer; however, Ishikawa discloses a passivation layer 3 on a top surface of an IC chip. It would have been obvious to include this layer on the top of the circuit layer (integrated circuit) 14 in the same manner as Ishikawa in order to protect the top circuits.

Regarding the applicant's argument that Hsiao in view of Sakaki does not teach or suggest all the claim limitations of the claimed invention, this argument is not persuasive because the references do indeed teach all of the claimed structural limitations. Hsiao discloses (see, for example, FIG. 1A) a semiconductor die comprising a substrate 100, devices (integrated circuit), and passivation layer 104/106. Hsiao does not disclose the stress balancing layer; however, Sakaki discloses a stress balancing layer 2 on a bottom surface of a substrate. It would have been obvious to include this layer on the bottom surface of the substrate in the same manner as Sakaki in order to prevent substrate warping.

Regarding the applicant's argument that Hsiao in view of Ouellet does not teach or suggest all the claim limitations of the claimed invention, this argument is not persuasive because the references do indeed teach all of the claimed structural limitations. Hsiao discloses (see, for example, FIG. 2b) a semiconductor die comprising a substrate 100, devices (integrated circuit), and passivation layer 104/106. Hsiao does not disclose the stress balancing layer; however, Ouellet discloses a stress balancing layer 3 on a bottom surface of a substrate. It would have been obvious to include this layer on the bottom surface of the substrate in the same manner as Ouellet in order to prevent substrate warping.

In response to applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on

Art Unit: 2815

obviousness is in any sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. In re McLaughlin, 443 F. 2d 1392; 170 USPQ 209 (CCPA 1971).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EUGENE LEE whose telephone number is (571)272-1733. The examiner can normally be reached on M-F 8-5.

Art Unit: 2815

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
December 23, 2008
/Eugene Lee/
Primary Examiner, Art Unit 2815